

REMARKS

Claims 1-9 are pending in the present application. Claims 1, 3 and 5-9 have been amended.

Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119. A certified copy of Japanese Priority Application No. 2001-246268 will be provided in due course.

Drawings

Applicant notes the Examiner's acceptance of the corrected drawings as filed along with the Amendment dated November 28, 2005.

Specification

As noted above, a certified copy of Japanese Priority Application No. 2001-246268 will be submitted in due course. Accordingly, the objection to the specification as asserted on page 3 of the previous Office Action dated July 26, 2005, should be held in abeyance.

The specification has been objected to as allegedly failing to provide proper antecedent basis for "mass of said impurity", as featured in claim 1. Claims 1-7 have been correspondingly objected to for these reasons.

Although Applicant does not necessarily concede that these objections to the specification and claims are proper, the claims have been amended to feature "an amount of said impurity". Although not necessarily limited thereto, antecedent basis for these features may be found on pages 11 and 12 of the specification, which describe an impurity amount that piles up in a cell. The Examiner is therefore respectfully requested to withdraw these objections for at least these reasons.

Claim Rejections-35 U.S.C. 112

Claims 1-8 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite. This rejection is respectfully traversed for the following reasons.

As emphasized in the Amendment dated November 28, 2005, the term mass is defined in Random House Webster's College Dictionary (1995) as "a body of coherent matter, usu. of indefinite shape: *a mass of dough*", or "a collection of incoherent particles, parts, or objects regarding as forming one body: *a mass of sand...*". By maintaining the rejection of claim 1, the Examiner has disregarded this definition and common usage of the term mass.

Although Applicant does not necessarily concede that this corresponding rejection of claim 1 under 35 U.S.C. 112, second paragraph is proper, claim 1 has been amended to feature "wherein an amount of said impurity in each of said cells moving to said impurity pileup portion from each of said cells is determined...". Claims 3 and 9 have been similarly amended. For instance, ΔC (x_i, y_i) is also described as an impurity

amount at the bottom of page 11 of the specification. Applicant respectfully submits that one of ordinary skill would readily understand the meaning of claim 1, particularly when taken in light of the specification. Applicant therefore respectfully submits that claim 1 is in compliance with 35 U.S.C. 112, second paragraph for at least these reasons.

Regarding claim 7, as described on page 21, lines 22-26 of the present application, the method may be carried out by an SOI process wherein the SI layer is sandwiched between a gate oxide film and a BOX insulating layer. Although not necessarily limited thereto, the "another insulating layer" of claim 7 may be interpreted as a BOX insulating layer. Applicants respectfully submit that claim 7 is in compliance with 35 U.S.C. 112, second paragraph.

With regard to claim 8, the Examiner has asserted that the source and drain process dependent parameters are vague. Claim 8 has been amended to provide values for λ_1 and λ_2 . Applicant therefore respectfully submits that claim 8 is in compliance with 35 U.S.C. 112, second paragraph.

Claim Rejections-35 U.S.C. 103

Claims 1-7 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Kumashiro reference (U.S. Patent No. 6,154,717) in view of the Lim et al. reference (Journal of Modeling and Simulation of Microsystems). This rejection is respectfully traversed for the following reasons.

As emphasized in the Amendment dated November 28, 2005, the method for modeling a semiconductor device process of claim 1 includes in combination “calculating the amount of said impurity included in each of said cells for each unit time after processing steps (a) through (f), wherein an amount of said impurity in each of said cells moving to said impurity pileup portion from each of said cells is determined as an impurity density as a function of a distance r_1 to said impurity pileup portion from each of said cells, and a function of a distance r_2 to said source or said drain from each of said cells”. Applicant respectfully submits that the prior art as relied upon by the Examiner does not make obvious these features.

The Examiner has asserted that the Kumashiro reference discloses all the features of claim 1, except for “setting data of a position of a source or a drain in said Si layer”. Although Applicant does not necessarily concede that the Kumashiro reference discloses all the other features of claim 1 as asserted by the Examiner, Applicant agrees that the Kumashiro reference does not disclose “setting data of a position of a source or a drain in said Si layer”. Consequently, since the Kumashiro reference does not disclose setting data of a position of a source or a drain, the Kumashiro reference also clearly fails to disclose calculating the amount of said impurity as further featured in claim 1. That is, the Kumashiro reference clearly does not determine an amount of impurity in each of the cells “as an impurity density as a function of distance r_1 to said impurity pileup portion from each of said cells, and a function of a distance r_2 to said source or said drain from each of said cells”.

In an effort to overcome the above noted deficiencies of the Kumashiro reference, the Examiner has alleged that the Lim et al. reference teaches source and drain edges contributing to the reverse short channel effect and thus affecting impurities. The Examiner has alleged that "It would be obvious necessity to know the position of source and drain. Further, LI 1999 teaches that the rate of diffusion for the impurities is shown to be function of two distances (LI 1999: Fig. 1 pg. 52, Equation 1-2)....". Applicant disagrees for the following reasons.

As emphasized beginning on page 17, line 11 of the Amendment dated November 28, 2005, equation (1) as described on page 52 of the Lim et al. reference is featured wherein y represents the distance across the channel and L_{eff} is the metallurgical channel length of the MOSFET. Clearly, these two distances y and L_{eff} do not respectively correspond to a distance r_1 "to said impurity pileup portion from each of said cells" and a distance r_2 "to said source or said drain from each of said cells", as would be necessary to meet the features of claim 1. That is, the above noted two distances y and L_{eff} in the Lim et al. reference are merely channel lengths of the MOSFET. These two distances are not described or even remotely suggested as distances from cells in an Si layer respectively to an impurity pileup portion and a source/drain.

In the Response To Applicant's Remarks section beginning on page 5 of the current Office Action dated February 27, 2006, the Examiner has agreed "that distances y and L_{eff} do not respectively correspond to distances r_1 and r_2 , as

would be necessary to meet the features of claim 1". In an apparent attempt to overcome this acknowledged deficiency of the Lim et al. reference, the Examiner has asserted that "however distances r1 and r2 as disclosed are another variation in looking at the relative position of the cell under consideration and would have been obvious to one skilled in the art once presented with the teachings of Li. Further, there are other possible variations like distance from the gate or embedded biasing electrodes used in the MOSFET design to correctly bias the N and P wells of the MOSFET".

Applicant respectfully submits that the reasoning behind the above noted arguments as presented by the Examiner is unclear, and in any event does not establish obviousness as would be necessary to meet the features of claim 1. As acknowledged by the Examiner, equation (1) of the Lim et al. reference features channel lengths y and L_{eff} , and these two distances do not correspond to distances r_1 and r_2 of claim 1. It would appear that the Examiner has taken the position that since equation (1) of the Lim et al. reference generally features two "distances", it would have been obvious to use any distances in equation (1), such as distances r_1 and r_2 from claim 1 for example. However, since the Lim et al. reference does not disclose distances r_1 and r_2 as acknowledged by the Examiner, this further position as apparently taken by the Examiner is completely improper and based solely on impermissible hindsight.

On page 5 of the current Office Action, the Examiner makes reference to "possible variations". Applicant respectfully submits that the Lim et al. reference does

not disclose "possible variations", and that it is unclear what such "possible variations" would be. Moreover, even if the Lim et al. reference disclosed such "possible variations", it is unclear how this would be relevant.

The Examiner has also asserted on page 5 of the current Office Action dated February 27, 2006 that although stated as channel lengths, distances y and L_{eff} of the Lim et al. reference "are related to impurity pileup portion defined by the terms N_{pile} and N_s ". Applicant respectfully respectfully submits that this particular argument as asserted by the Examiner is unclear. Although lengths y and L_{eff} may be terms of equations (1) and (2) of the Lim et al. reference, these terms y and L_{eff} are merely channel lengths. Regardless of what other terms are present in equations (1) and (2), as previously acknowledged by the Examiner, distances y and L_{eff} do not correspond to distances r_1 and r_2 of claim 1. Thus, any assertion that distances r_1 and r_2 would have been obvious clearly can not be based on the relied upon prior art, and thus must be based on impermissible hindsight.

Applicant therefore respectfully submits that the Lim et al. reference as relied upon by the Examiner does not overcome the acknowledged deficiencies of the primarily relied upon the Kumashiro reference. Accordingly, Applicant respectfully submits that the method for modeling a semiconductor device process of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 1-7 is improper for at least these reasons.

Regarding claim 2, since the prior art as relied upon by the Examiner does not disclose distances that correspond to distances r1 and r2 of claim 1, the prior art as combined clearly fails to disclose or make obvious the features of claim 2.

The Examiner has apparently relied upon Official Notice to assert that the features of claim 3 would have been obvious. Applicant respectfully challenges the Examiner's use of Official Notice. The Examiner is respectfully requested to provide a corresponding prior art reference that teaches the features of claim 3.

Regarding claim 5, since the prior art as relied upon by the Examiner does not set data of a position of a source or a drain, and does not disclose distances r1 and r2 as featured in claim 1, the prior art as relied upon clearly fails to disclose or make obvious the features of claim 5.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

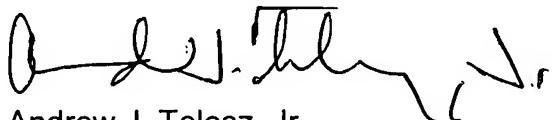
In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Serial No. 10/059,176
OKI.298
Amendment dated May 30, 2006

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



Andrew J. Telesz, Jr.
Registration No. 33,581

One Freedom Square
11951 Freedom Drive, Suite 1260
Reston, Virginia 20190
Telephone No.: (571) 283-0720
Facsimile No.: (571) 283-0740